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AN ANALYTICAL APPROACH TO DESIGN VLSI IMPLEMENTATION OF LOW POWER, HIGH SPEED SRAM CELL USING SUB-MICRON TECHNOLOGY

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Abstract

The present title discloses a design and analysis of high speed Static Random Access Memory (SRAM) cell to develop low power consumption. The Low-Power and High-performance CMOS devices are an industry needs these days. Among the various embedded memory technologies, SRAM is able to provide the highest performance while maintaining low standby power consumption.

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SRAM cells have been the predominant technologies used to implement memory cells in computer systems, each one having its advantages and shortcomings. SRAM cells are faster and require no refresh since reads are not destructive. Here we use SRAM cell built from a simple static latch and tri state inverter. The reading action itself refreshes the content of memory. The SRAM access path is split into two portions: from address input to word line rise (the row decoder) and from word line rise to data output (the read data path). The decoder which constitutes the path from address input to the word line rise is implemented as a binary structure by implementing a multi-stage path. The key to low power operation in the SRAM data path is to reduce the signal swings on the high capacitance nodes like the bit lines and the data lines.

The goal of this paper is to reduce the power and area of the Static Random Access Memory (SRAM) array while maintaining the competitive performance. Here the various configuration of SRAM array is designed using both the Twelve-transistor (12T) SRAM cell and a six-transistor (6T) SRAM cell in deep submicron CMOS technologies. Compared to the conventional 12T SRAM array, the load less 6T SRAM array consumes less power with less area in deep submicron CMOS technologies.

Keywords –12-T SRAM cell, loadless 6T SRAM cell, Low power, SRAM

I. Introduction

Static Random Access Memories (SRAM) has been the predominant technologies used to implement memory cells in computer systems. SRAM cells, typically implemented with six transistors (6T cells) have been usually designed for speed. Cache memories occupy an important percentage of the overall die area. A major drawback of these memories is the amount of dissipated static energy or leakage, which is proportional to the number of transistors used to implement these structures. The on-chip caches in embedded microprocessors are implemented using arrays of densely packed Static Random Access Memory (SRAM) cells. The number of transistors devoted to the on-chip caches is often a significant fraction of the total transistors devoted for the entire chip. According to International Technology Roadmap for Semiconductors (ITRS)-2005, SRAM is going to occupy more than 60% of the System-on-Chips (SoCs) in the future. Thus reducing the number of transistors in the basic cell leads to the overall reduction in the number of transistors in the SRAM array and thus leading to the overall reduction in the area occupancy of the SRAM array. A few critical circuits in a system not only affect the design metrics but may fail to operate in deep submicron technology. Hence the SRAM arrays are designed, analyzed and checked for its design metrics in deep submicron CMOS technologies.

Two types of SRAM cells will be considered in this paper. (i) Conventional Twelve-transistor (12T) SRAM cell, as shown in Figure 1. (ii) Loadless six-transistor (6T) SRAM Cell, as shown in Figure 3. They will be designed and analyzed in various configurations with respect to functionality, power dissipation, area occupancy, stability and access time.

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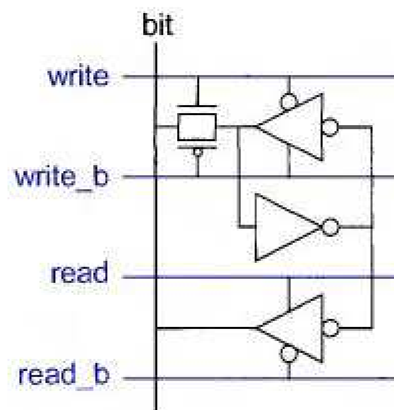

Fig 1: 12-transistor SRAM cell

The fundamental building block of a static RAM is the SRAM memory cell. The cell is activated by raising the word line and is read or written through the bit line. Fig (1) shows a 12-transistor SRAM cell built from a simple static latch and tri-state inverter. The cell has a single bit line. True and complementary read and write signals are used in place of a single word line. A representative layout in Fig (2) has an area of 46 x 75 X. The power and ground lines can be shared between mirrored adjacent cells, but the area is still limited by the wires and is undesirably large. However, the cell is easy to design because all nodes swing rail-to-rail and it is fast when used in small RAMs and register files. Fig (3) shows a 6-transistor (6T) SRAM

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commonly used in practice. Such a cell uses a single word line and both true and complementary bid lines. The complementary bit- line is often called bit or bit. The cell contains a pair of crosscoupled inverters and an access transistor for each bit line. True and complementary versions of the data are stored on the cross-coupled inverters. If the data is disturbed slightly, positive feedback around the loop will restore it to VDD or GND. The word line is asserted to read or write the cell.

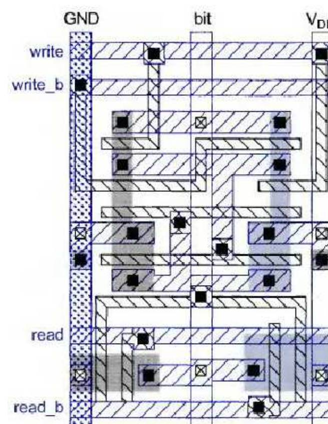

Fig 2: Representative layout of 46 x 75 X

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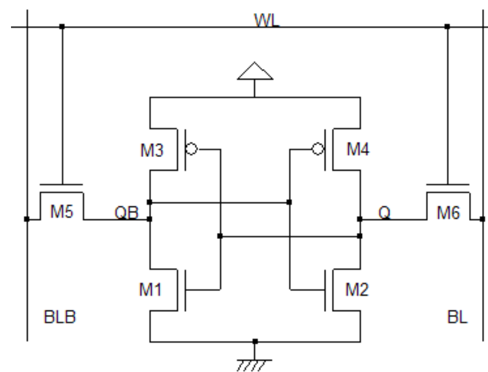

Fig 3: Conventional 6T SRAM Cell.

A 6T SRAM cell consists of two cross-coupled inverters (M1-M3 and M2-M4) forming a latch and the access transistors (M5 and M6). In the new loadless 4T SRAM cell, two NMOS transistors (M3 and M4) are used as pass transistors to access the cell and two PMOS transistors (M1 and M2) are used as drivers for the cell. An SRAM cell must be designed such that it provides a non-destructive read operation and a reliable write operation. The working of the new loadless 4T SRAM cell can be found in [3] and the conventional 6T SRAM cell can be found in [4-9].

II. Precharge Circuits

The precharge circuit used for the new loadless 6T SRAM array is different from that of the 12T SRAM array. The function of the precharge circuit in the 12T SRAM array is to charge the Bit Line (BL) and Bit Line Bar (BLB) to VDD. In the new loadless 6T SRAM array the bitlines are precharged to ground instead of VDD and thus consuming less power than the 6T SRAM

array. The schematic of the pre-charge circuit for the 12T SRAM array is shown in Figure. 4(a) and that of the new loadless 6T SRAM array is shown in Figure. 4(b). The Precharge (PC) signal enables the bit-lines to be pre-charged at all times except during write and read cycle. The transistor M1 and M2 will precharge the bitlines while the transistor M3 will equalize them to ensure both bit lines within a pair are at the same potential before the cell is read. The same circuit topology is used for local precharge in combination with the SA in the corresponding SRAM arrays.

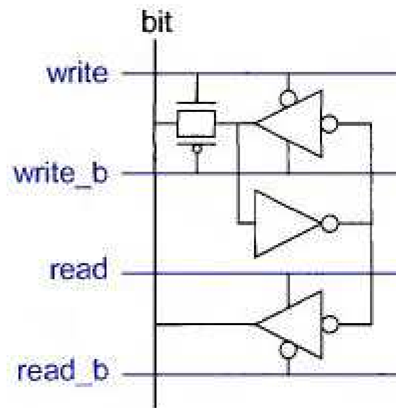

Fig 4(a): Conventional 12T SRAM Cell.

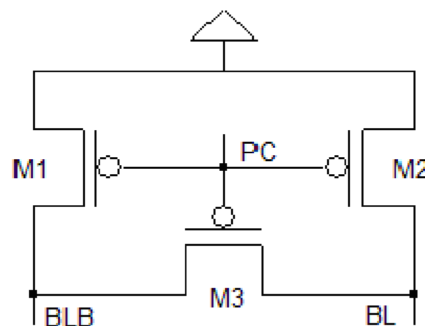

Fig 4(b): Conventional 6T SRAM Cell.

III. Memory Architecture

The preferred organization for Random access memories is shown in Fig 5. This organization is random-access architecture which is an Asynchronous design. The name is derived from the fact that memory locations (addresses) can be accessed in random order at a fixed rate, independent of physical location, for reading or writing. The storage array, or core, is made up of simple cell circuits arranged to share connections in horizontal rows and vertical columns. The horizontal lines, which are driven only from outside the storage array, are called word lines, while the vertical lines, along which data flow into and out of cells, are called bit lines. A cell is accessed for reading or writing by selecting its row and column. Each Cell can store 0 or 1.

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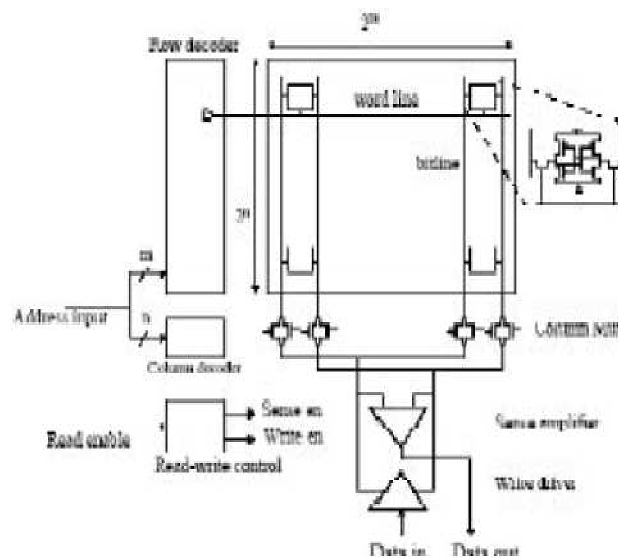

Fig 4: SRAM Memory Architecture

Memories may simultaneously select 4, 8, 16, 32, or 64columns in one row depending on the application. The row and column (or groups of columns) to be selected are determined by decoding binary address information. In this design, the number of rows and columns, both are equal to 64 for 4Mb memory cut. Using two such memory cuts, a 8Mb SRAM memory is designed.

IV. Simulation Environment and Results

The following configuration of SRAM arrays were designed and analyzed using the conventional 6T SRAM Cell and the New Loadless 12T SRAM Cell: (a) 1*1 (b) 16*16 (c) 32*32.

The various configurations were simulated using HSPICE, using the Nominal Predictive Technology Model (PTM) in 130nm, 90nm and 65nm CMOS technologies. The functionality of 1*1 6T SRAM cell is shown in Figure. 5 and that of 1*1 New Loadless 4T SRAM cell is shown in Figure. 6

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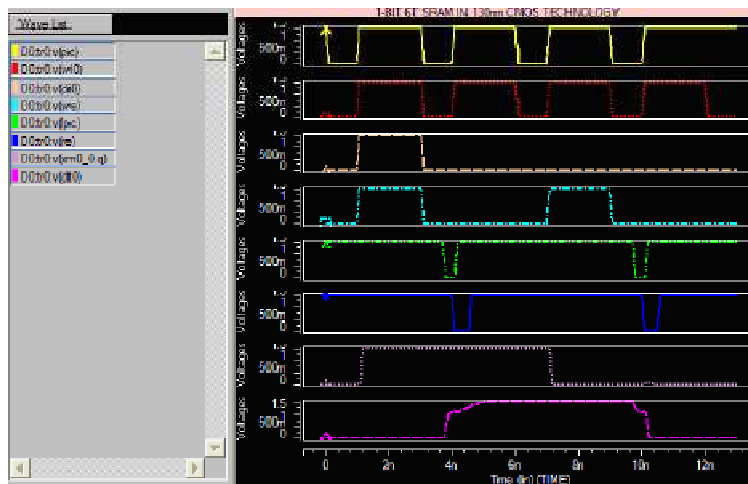
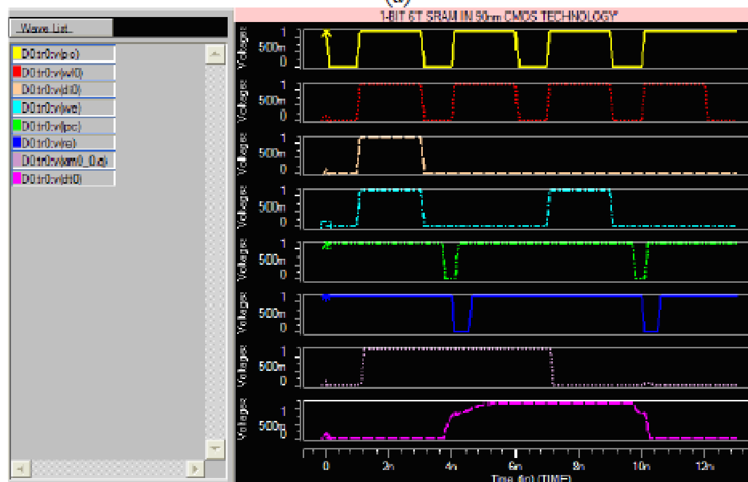
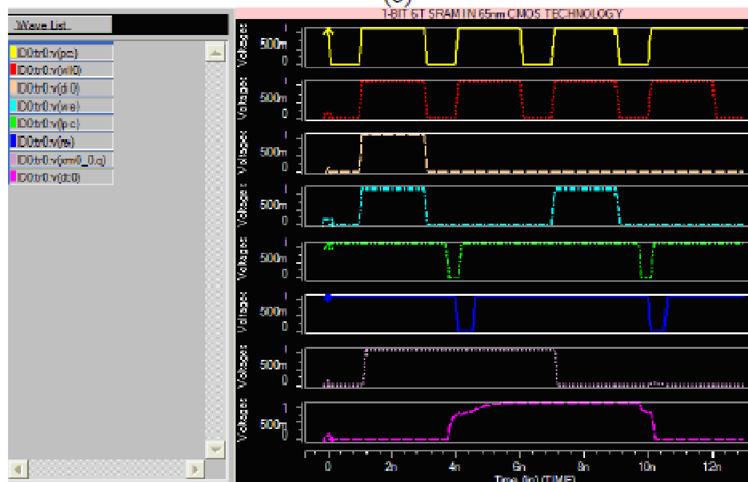


(a)



(b)



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(c)

Figure 5. Write-Read Cycle of 1-Bit 6T SRAM. (a) In 130nm CMOS Technology. (b) In 90nmCMOS Technology. (c) In 65nm CMOS Technology.

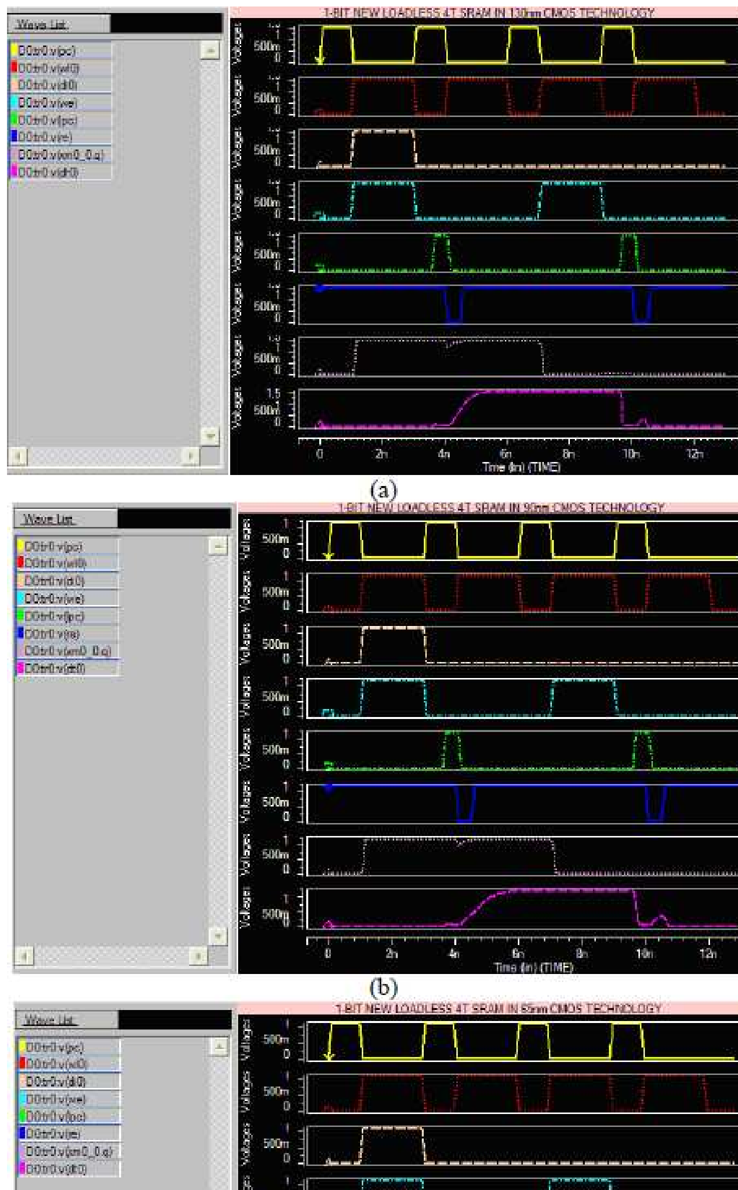

Figure 6. Write-Read Cycle of 1-Bit New Loadless 4T SRAM. (a) In 130nm CMOS Technology. (b) In 90nm CMOS Technology. (c) In 65nm CMOS Technology.

The frequency at which the both the cells were made to operate was 333.33MHz. Each bitlines was assumed to have a capacitance of 20fF. Also a load of 20fF was connected to each output line of SA. Similar procedure was used to check the functionality for other configurations of both the types of SRAM arrays in all the CMOS technologies.

V. Conclusion

The New Load less 12T-SRAM cell is designed and analyzed in deep submicron (130nm, 90nm and 65nm) CMOS technologies, which establish the technology independence of the New Load less 6T SRAM cell and its consistent performance with respect to Conventional 12T SRAM cell in deep sub-micron regime. The New Load less 12T SRAM array consumes low power with low area. The most significant feature of this new load less 6T SRAM Cell is that there is no need to modify any of the fabrication process. Thus it can be used for on chip caches in embedded microprocessors, high density SRAMs embedded in any logic devices, as well as for stand-alone SRAM applications.

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